Shwetha Shankar

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Ph.D. researcher with an 18+ year background in software engineering and semiconductor industry, seeking to integrate extensive industry expertise into university-level teaching. Looking for academic teaching positions to gain formal instructional experience while offering students practical insight into modern industry practices and engineering challenges.

➢ EDUCATION

- **Doctor of Philosophy in Computer Science** (Texas State University, San Marcos) – Current GPA 3.80/4 [**Expected 2028**]
  - Coursework: High Performance Computing, HPC@Scale, Advanced Data Mining, Machine Learning, Mobile Network and Computing.
  - PhD Research Focus: Developing high-performance machine learning frameworks to analyze complex healthcare datasets. Utilizing HPC architectures to scale multi-modal clustering algorithms, optimize high-dimensional data pipelines, and improve computational efficiency in medical AI applications.

- **Master's (Thesis) in Computer Science** (Texas State University, San Marcos) – GPA 3.89/4 [**Jun '10 – Dec '12**]
  - Coursework: Operating Systems, Artificial Intelligence, Software Engineering, Multimedia Computing, Algorithm & Design, Java & Design of Programming languages, Networks and Communication, Parallel Processing.
  - Master's Thesis : Designed an OS task scheduling policy for homogeneous multi-core architectures to optimize performance while balancing power metrics across cores. Implemented a C++ discrete-time event CPU simulator utilizing advanced work-stealing algorithm variants to evaluate and balance scheduling policies against strict power envelopes
  - Bridge Certificate Program in Computer Science (Texas State University).
    - Coursework: C/C++, Data Structures, Digital Logic, Computer Architecture, Assembly Language

- **Bachelor of Engineering – Industrial Engineering and Management** **[Oct '00 – Jul '04]**
  - Graduated with First Class Distinction at Visvesvaraya Technological University, Karnataka, India.

➢ PUBLICATIONS

- "Power Aware Work Stealing in Homogenous Multi-Core Systems," The Sixth International Conference on Computational Technologies and Applications, Venice, Italy, May 2014, pp. 30-38
- "Towards an OS-Centric Framework for Energy Efficient Scheduling of Parallel Workloads," PPTDA-2013, The 2013 International Conference on Parallel and Distributed Processing Techniques and Applications, Las Vegas, U.S., July 2013

➢ TEACHING EXPERIENCE

- Guest Lecturer
  - CS 3339: Computer Architecture Basics [Spring 2026]

➢ REFERENCES: Available on request

➢ WORK PERMIT: Permanent Resident (Green Card holder). No sponsorship required.

WORK EXPERIENCE

Server Performance Architect **[Mar 2018 – Mar 2026]**
Intel Corporation (Austin, Texas)

- Model Feature Engineering: Modeled architectural features (opcode flows, dynamic throttling, scheduling, and routing policies) within a C++ server uncore performance model, ensuring high-fidelity architectural alignment and valid performance projections.
- Mesh Optimization & Tuning: Improved pre-silicon mesh performance by 5% to 15% across multiple server SoCs by debugging complex mesh hotspots, balancing routing, and resolving buffer bottlenecks via detailed model simulations.
- Performance & Area Analysis: Conducted targeted simulation studies to determine optimal register settings for new features and identified fabric IP redundancies to optimize buffer sizing and hardware area footprints.

Pre-Silicon Performance Validation Engineer **[Mar 2015 – Feb 2018]**
Intel Corporation (Austin, Texas)

- Emulation & Counter Validation: Led pre-silicon validation and debugging of performance monitoring counters in mobile SoCs to establish critical telemetry frameworks for hardware tuning.
- Display IP Verification: Validated Display IP bandwidth, QoS mechanisms, buffer thresholds, and MMUs, resolving critical register configuration bugs and validation coverage gaps.
- Cross-Platform Porting: Ported verification tests and emulation scripts directly to post-silicon platforms, ensuring seamless environment transitions and accelerating debug timelines.

Post-Silicon Performance Validation Engineer **[Mar 2013 – Feb 2015]**
Intel Corporation (Austin, Texas)

- Subsystem Silicon Debug: Validated Core-to-Memory and Display IP performance on Intel Atom projects, debugging complex firmware mismatches, clock initializations, and BGF delay programming bugs.
- Benchmarking & Telemetry: Conducted performance characterization using synthetic benchmarks and telemetry tools (PMUs, VISA, Logic Analyzers, SOCWatch, SEP) to deliver optimal power/performance tuning matrices.
- Accelerated Validation: Cut the 22nm mobile SoC validation lifecycle to a record two quarters from tape-in to PRQ by leveraging test automation and $n-1$ emulation platforms.

Programmer Analyst **[July 2004 – Mar 2010]**
Infosys Technologies Ltd (Bangalore, India)

- Worked for Fidelity Investments (on-site) to develop and support end-to-end JAVA/BLAZE based proprietary software solutions to calculate the defined retirement benefits of their clients' employees. Involved in complex software customizations for each new client.
- Responsible for successfully completing 4 new client implementations and 6 enhancement projects.

Awards

Intel Corporation (2013 – 2026)

- **Division Recognition Award:** Automated the critical mesh performance configuration, setup, and validation flow, significantly reducing pre-silicon performance validation timelines and improving deliverable quality across multiple server products.
- **Division Recognition Award:** Implemented a novel x86 ISA opcode in the uncore performance model; conducted extensive simulation and data analysis to determine the optimal buffer size required to maximize hardware performance.
- **System Validation Group Excellence Award:** Recognized for a rapid engineering ramp-up from post-silicon to emulation platforms, successfully delivering all pre-silicon performance validation milestones on schedule.
- **Division Recognition Award:** Enhanced mobile SoC display IP silicon performance through cross-functional collaboration, identifying hardware stress failure points, and delivering optimal hardware tuning and software driver recommendations.

Texas State University (2010- 2013)

- Graduate Academic Excellence Award, 2012.
- Graduate Research Excellence Award, 2012.
- Graduate Research Excellence Award, 2013.