TEXAS STATE VITA

I. Academic/Professional Background

A. Name and Title

Name: Dr. Martin Burtscher Title: Professor

B. Educational Background

Degree	*Year*	*University*	*Major*	*Thesis/Dissertation*
PHD	2000	University of Colorado Boulder	Computer Science	
MSC	1996	Swiss Fed Inst of Technology	Computer Science Engineering	

D. Relevant Professional Experience

Position	*Entity*	*Comments*	*Dates*
Professor	Texas State University		September 2015 - Present
Associate Professor	Texas State University		August 2010 - August 2015
Research Scientist	The University of Texas at Austin		August 2007 - August 2010
Assistant Professor	Cornell University		July 2000 - June 2007

II. TEACHING

A. Teaching Honors and Awards:

Award / Honor Recipient: Teaching Award of Honor, Alumni Association.
August 2020

Award / Honor Recipient: Alpha Chi Favorite Professors for 2016, Alpha Chi National Honor Society.
November 2016

Award / Honor Recipient: GPU Education Center Renewal, NVIDIA Corporation.
March 2016

Award / Honor Recipient: Alpha Chi Favorite Professors for 2015, Alpha Chi National Honor Society.
November 2015

Award / Honor Recipient: Alpha Chi Favorite Professors for Spring 2014, Alpha Chi National Honor Society.
March 2014

Award / Honor Recipient: CUDA Teaching Center Award, NVIDIA Corporation.
2012

Award / Honor Recipient: College Achievement Award for Excellence in Teaching, College of Science and Engineering, Texas State University-San Marcos.
August 2012

Award / Honor Recipient: Michael Tien ’72 Excellence in Teaching Award, Cornell University.
2003

Award / Honor Recipient: Third Annual Teaching Effectiveness Award (honorable mention), University of Colorado at Boulder.
1998

B. Courses Taught:

Texas State University:

CS 1428 - FOUNDATNS OF CS I

CS 3339 - COMPUTER ARCHITECT

CS 3358 - DATA STRUCTURES

CS 4298 - UNDERGRAD RSRCH I

CS 4299 - UNDERGRAD RSRCH II

CS 4378T - PARALLEL PROGRMNG

CS 4380 - PARALLEL PROGRAMNG

CS 4395 - INDEPENDENT STUDY

CS 5199B - THESIS

CS 5299B - THESIS

CS 5348 - COMP ORG & DESIGN

CS 5351 - PARALLEL PROCESSIN

CS 5351 - PARALLEL PROCESSING

CS 5395 - IND STUDY ADV

CS 5399A - THESIS

CS 5399B - THESIS

CS 5599B - THESIS

CS 5999B - THESIS

CS 7332 - ADVANCED PARALLEL COMPUTING

CS 7387 - RESEARCH IN COMPUTER SCIENCE

CS 7399 - DISSERTATION

CS 7699 - DISSERTATION

CS 7999 - DISSERTATION

Department of Computer Science, University of Colorado at Boulder:

CSCI 2270 - Data Structures and Algorithms

Department of Computer Sciences, The University of Texas at Austin:

CS 378 - Programming for Performance

School of Electrical and Computer Engineering, Cornell University:

ECE 473 - Optimizing Compilers

ECE 475 - Computer Architecture

ECE 575 - High-Performance Microprocessor Architecture

ECE 697 - Topics in Computer Systems

ENGRG 150 - Engineering Seminar

C. Directed Student Learning (i.e. theses, dissertations, exit committees, etc.):

Supervisor / Chair, Master's Thesis, "Parallelizing a Greedy TSP Algorithm", Status: Completed. (December 2020). CS.
Student(s): Andres Gonzalez, Graduate.

Supervisor / Chair, Master's Thesis, "Increasing the Parallelism of Graph Algorithms", Status: Completed. (December 2020). CS.
Student(s): Jarim Seo, Graduate.

Supervisor / Chair, Master's Thesis, "Out-of-core Graph Algorithms on the GPU", Status: Completed. (August 2020). CS.
Student(s): Yiqian Liu, Graduate.

Supervisor / Chair, Master's Thesis, "Parallelizing Pattern Routing Algorithms for Chip Design", Status: Completed. (May 2020). CS.
Student(s): Aarti Kothari, Graduate.

Supervisor / Chair, Applied Research Project, "Communication Reduction in Irregular Computations", Status: Completed. (2017).
Student(s): Dean Terrell, Undergraduate.

Supervisor / Chair, Applied Research Project, "Minimum Spanning Tree Algorithms for GPUs", Status: Completed. (2017).
Student(s): Randy Cornell, Undergraduate.

Supervisor / Chair, Independent Study, "Optimization and Performance Analysis of P2P Direct Communication in a Multi-GPU Irregular Program", Status: Completed. (2017). CS.
Student(s): Sahar Azimi, Graduate.

Supervisor / Chair, Master's Thesis, "Data-Transformation Algorithms for Minimizing Bit Flips on GPU Data Buses", Status: Completed. (August 2017). CS.
Student(s): Arthi Nagarajan, Graduate.

Supervisor / Chair, Master's Thesis, "An Efficient Connected Components Algorithm for Massively-Parallel Devices", Status: Completed. (May 2017). CS.
Student(s): Jayadharini Jaiganesh, Graduate.

Supervisor / Chair, Master's Thesis, "GPU Execution Tracing and Compression", Status: Completed. (May 2017). CS.
Student(s): Sahar Azimi, Graduate.

Supervisor / Chair, Honor's Thesis, "Multi-GPU Acceleration", Status: Completed. (December 2016). CS.
Student(s): Kristi Belcher, Undergraduate.

Member, Master's Thesis, "Understanding the Impact of Hybrid Programming on Software Energy Efficiency", Status: Completed. (August 2016). CS.
Student(s): Donna Lakomski, Graduate.

Member, Master's Thesis, "Dynamic Unbounded Integer Compression", Status: Completed. (August 2016). CS.
Student(s): Naga Sai Gowtham Mulpuri, Graduate.

Member, Master's Thesis, "Using the Greenup, Powerup and Speedup Metrics to Evaluate Software Energy Efficiency", Status: Completed. (August 2016). CS.
Student(s): Sarah Abdulsalam, Graduate.

Supervisor / Chair, Master's Thesis, "Higher-Order and Tuple-Based Massively-Parallel Prefix Sums", Status: Completed. (May 2016). CS.
Student(s): Sepideh Maleki, Graduate.

Supervisor / Chair, Master's Thesis, "Low-Overhead Tracing of Large-Scale Parallel Programs", Status: Completed. (May 2016). CS.
Student(s): Sindhu Devale, Graduate.

Member, Master's Thesis, "Energy Efficiency Analysis and Optimization of Convolutional Neural Networks for Image Recognition", Status: Completed. (May 2016). CS.
Student(s): Xinbo Chen, Graduate.

Supervisor / Chair, Applied Research Project, "Effective Compression Algorithms for Massively-Parallel Architectures", Status: Completed. (2015).
Student(s): Annie Yang, Undergraduate.

Supervisor / Chair, Applied Research Project, "Optimizations to Improve Energy Efficiency", Status: Completed. (2015).
Student(s): Jared Coplin, Undergraduate.

Supervisor / Chair, Independent Study, "Parallelization and Optimization of the Maximal Independent Set Problem", Status: Completed. (2015). CS.
Student(s): Sindhu Devale, Graduate.

Supervisor / Chair, Master's Thesis, "Unobtrusive Real-time Tracing of Parallel Programs", Status: Completed. (May 2015). CS.
Student(s): Farbod Hesaaraki, Graduate.

Supervisor / Chair, Master's Thesis, "Universal Strategies for Accelerating Irregular Codes Using GPUs", Status: Completed. (May 2015). CS.
Student(s): Molly A. O'Neil, Graduate.

Member, Master's Thesis, "An Exploration into the Effectiveness of Prefetching on Program Performance with the Help of an Autotuning Model", Status: Completed. (May 2015). CS.
Student(s): Saami Rahman, Graduate.

Member, Master's Thesis, "HASTE: A Heterogeneously Accelerated SQL Transaction Engine", Status: Completed. (December 2014). CS.
Student(s): Brian Romoser, Graduate.

Member, Master's Thesis, "Dynamic Feedback-Driven Thread Migration for Energy-Efficient Execution of Multithreaded Workloads", Status: Completed. (December 2014). CS.
Student(s): Claudia Alvarado, Graduate.

Supervisor / Chair, Master's Thesis, "Automatically Synthesizing Effective Data Compression and Decompression Algorithms", Status: Completed. (December 2014). CS.
Student(s): Hari Mukka, Graduate.

Supervisor / Chair, Master's Thesis, "Automatic Optimization Suggestions for GPU Programs", Status: Completed. (December 2014). CS.
Student(s): Saeed Taheri, Graduate.

Supervisor / Chair, Independent Study, "OpenCL on the GPU: A Case Study of Graph Cuts for Image Segmentation", Status: Completed. (2012). CS.
Student(s): James Shockey, Graduate.

Member, Master's Thesis, "Exploiting Shared-Memory Reuse through Source-Level Transformation of CUDA Kernels", Status: Completed. (December 2011). CS.
Student(s): Swapneela Unkule, Graduate.

Supervisor / Chair, Dissertation, "Efficient Runtime Detection and Toleration of Asymmetric Races", Status: Completed. (August 2009). ECE.
Student(s): Paruj Ratanaworabhan, Doctoral.

Supervisor / Chair, Dissertation, "Using General-Purpose Processor Cores as Prefetching Engines in Chip Multiprocessor Architectures", Status: Completed. (August 2007). ECE.
Student(s): Ilya Ganusov, Doctoral.

Member, Dissertation, "A Workload Adaptive Voltage Scaling Multiple Clock Domain Architecture", Status: Completed. (January 2007). ECE.
Student(s): David Biermann, Doctoral.

Member, Dissertation, "Characterization and Application of Advanced VLSI Interconnects", Status: Completed. (January 2007). ECE.
Student(s): Weiping Ni, Doctoral.

Member, Dissertation, "Implementing Self-healing Behavior in Quasi Delay Insensitive Circuits", Status: Completed. (August 2006). ECE.
Student(s): Song Peng, Doctoral.

Supervisor / Chair, Master's Thesis, "Design and Evaluation of Multiple Branch Execution Paths in Out-of-order Superscalar Microprocessor Architectures", Status: Completed. (May 2006). ECE.
Student(s): Kevin Oh, M.Eng.

Member, Dissertation, "On the Role of Search in Generating High-Performance BLAS Libraries", Status: Completed. (January 2006). CS.
Student(s): Kamen Yotov, Doctoral.

Supervisor / Chair, Master's Thesis, "Self-optimizing Finite State Machines for Confidence Estimators", Status: Completed. (January 2006). ECE.
Student(s): Sandra J. Jackson, Graduate.

Supervisor / Chair, Master's Thesis, "Hardware Prefetching based on Future Execution in Chip Multiprocessor Architectures", Status: Completed. (August 2005). ECE.
Student(s): Ilya Ganusov, Graduate.

Member, Dissertation, "BitSNAP: A Low-Energy Sensor Network Asynchronous Processor with Dynamic Significance Compression", Status: Completed. (May 2005). ECE.
Student(s): Virantha N. Ekanayake, Doctoral.

Supervisor / Chair, Master's Thesis, "A New Latency-based Predictive Cache Allocation Scheme", Status: Completed. (May 2005). ECE.
Student(s): Edward Lo, M.Eng.

Member, Dissertation, "Fast Prototyping of Asynchronous Logic", Status: Completed. (August 2004). ECE.
Student(s): John R. Teifel, Doctoral.

Supervisor / Chair, Master's Thesis, "A Real-Time Development Framework for the ASTRO VTVL Vehicle", Status: Completed. (May 2003). ECE.
Student(s): Jacky Cheung, M.Eng.

Supervisor / Chair, Master's Thesis, "A Configurable MIPS Processor Simulator", Status: Completed. (May 2003). ECE.
Student(s): Sriram Chandrasekar, M.Eng.

Supervisor / Chair, Master's Thesis, "A Configurable MIPS Processor Simulator", Status: Completed. (May 2003). ECE.
Student(s): Vishal Salvi, M.Eng.

Supervisor / Chair, Master's Thesis, "Type-based Load-Value Prediction", Status: Completed. (January 2003). ECE.
Student(s): Nana B. Sam, Graduate.

Supervisor / Chair, Master's Thesis, "Trace-File Compression Using Value-Prediction Techniques", Status: Completed. (August 2002). ECE.
Student(s): Metha Jeeradit, M.Eng.

Supervisor / Chair, Master's Thesis, "Branch Prediction with Feedforward Neural Networks", Status: Completed. (August 2002). ECE.
Student(s): Paruj Ratanaworabhan, M.Eng.

Supervisor / Chair, Master's Thesis, "An Investigation of the Load-Value Predictability of Commonly used Algorithms", Status: Completed. (August 2002). ECE.
Student(s): Weiwei Zhang, M.Eng.

Supervisor / Chair, Master's Thesis, "Constructing a Bus Traffic Monitoring System to Evaluate the Data Predictability using the ATOM Tool-Kit", Status: Completed. (May 2001). ECE.
Student(s): Jintadhee Sudasna, M.Eng.

Supervisor / Chair, Master's Thesis, "Potential of Load Value Predictors Working with Caches", Status: Completed. (January 2001). CS.
Student(s): Jangwoo Kim, M.Eng.

D. Courses Prepared and Curriculum Development:

Advanced Parallel Computing, New Course: 2018.

Additional Comments: 3 credit hours, PhD course

Parallel Programming, New Course: 2011.
Additional Comments: 3 credit hours, senior course

Optimizing Compilers, New Course: 2003.
Additional Comments: 4 credit hours, senior course

Computer Architecture, New Course: 2002.
Additional Comments: 4 credit hours, senior course converted to Curriculum Major Design Experience course to meet ABET requirements

High-Performance Microprocessor Architecture, New Course: 2001.
Additional Comments: 4 credit hours, graduate course

Topics in Computer Systems, New Course: 2000.
Additional Comments: 1 credit hour, graduate seminar

F. Other:

Certification, Teaching Online @ TxState course (meets SACSCOC requirements for online instructors). (July 2020).

Student Accomplishments:

Award:

Mentor, Conference of Southern Graduate School (CSGS) Outstanding Master's Thesis Award in Math, Physical Sciences and Engineering. (2017).
Student(s): Sepideh Maleki, Graduate, MS.

Mentor, Graduate College's Outstanding Master's Thesis Award in Mathematics, Physical Sciences, and Engineering. (2016).
Student(s): Sepideh Maleki, Graduate, MS.

Mentor, CRA 2016 Outstanding Undergraduate Researcher Award. (2016).
Student(s): Jared Coplin, Undergraduate, BS.

III. SCHOLARLY/CREATIVE

A. Works in Print (including works accepted, forthcoming, in press):

1. Books:

d. Chapters in Books:

Refereed:

Dzhagaryan, A., Milenkovic, A., & Burtscher, M. (2016). Improving the Effectiveness of Data Transfers in Mobile Computing Using Lossless Compression Utilities. In *Advances in Computer Communications and Networks* (pp. 181–221). River Publishers.

Coplin, J., & Burtscher, M. (2016). Energy and Power Considerations of GPUs. In *Advances in GPU Research and Practice* (pp. 509–541). Elsevier.

Yang, A., Coplin, J., Mukka, H., Hesaaraki, F., & Burtscher, M. (2016). MPC: An Effective Floating-Point Compression Algorithm for GPUs. In *Advances in GPU Research and Practice* (pp. 327–347). Elsevier.

Burtscher, M., & Pingali, K. (2011). An Efficient CUDA Implementation of the Tree-based Barnes Hut n-Body Algorithm. In *GPU Computing Gems Emerald Edition* (pp. 75–92).

2. Articles:

a. Refereed Journal Articles:

Burtscher, M., Devale, S., Azimi, S., Jaiganesh, J., & Powers, E. (2018). A High-Quality and Fast Maximal Independent Set Implementation for GPUs. *ACM Transactions on Parallel Computing*, *5*. Published.

Szczyrba, I., Szczyrba, R., & Burtscher, M. (2016). Geometric Representations of the n-anacci Constants and Generalizations Thereof. *Journal of Integer Sequences*, *19*. Published. Retrieved from <https://cs.uwaterloo.ca/journals/JIS/VOL19/Szczyrba/sz4.pdf>

Szczyrba, I., Szczyrba, R., & Burtscher, M. (2015). Analytic Representations of the n-anacci Constants and Generalizations Thereof. *Journal of Integer Sequences*, *18*. Published. Retrieved from https://cs.uwaterloo.ca/journals/JIS/VOL18/Szczyrba/sz3.pdf

Li, B., Lu, Y., Li, C., Godil, A., Schreck, T., Aono, M., … Zou, C. (2015). A Comparison of 3D Shape Retrieval Methods based on a Large-Scale Benchmark Supporting Multimodal Queries. *Computer Vision and Image Understanding*, *131*, 1–27.

Uzelac, V., Milenkovic, A., Milenkovic, M., & Burtscher, M. (2014). Using Branch Predictors and Variable Encoding for On-the-Fly Program Tracing. *IEEE Computer Society*, *63*, 1008–1020.

Ratanaworabhan, P., Burtscher, M., Kirovski, D., Zorn, B., Nagpal, R., & Pattabiraman, K. (2012). Efficient Runtime Detection and Toleration of Asymmetric Races. *IEEE Computer Society*, *61*, 548–562.

Milenkovic, A., Uzelac, V., Milenkovic, M., & Burtscher, M. (2011). Caches and Predictors for Real-time, Unobtrusive, and Cost-Effective Program Tracing in Embedded Systems. *IEEE Computer Society*, *60*, 992–1005.

Burstedde, C., Burtscher, M., Ghattas, O., Stadler, G., Tu, T., & Wilcox, L. C. (2009). ALPS: A Framework for Parallel Adaptive PDE Solution. *Journal of Physics: Conference Series*, *180*. Published. Retrieved from http://www.iop.org/EJ/toc/1742-6596/180/1

Burtscher, M., & Ratanaworabhan, P. (2009). FPC: A High-Speed Compressor for Double-Precision Floating-Point Data. *IEEE Transactions on Computers*, *58*, 18–31.

Ganusov, I., & Burtscher, M. (2006). Future Execution: A Prefetching Mechanism that Uses Multiple Cores to Speed up Single Threads. *ACM Transactions on Architecture and Code Optimization*, *3*, 424–449.

Liu, C. C., Ganusov, I., Burtscher, M., & Tiwari, S. (2005). Bridging the Processor-Memory Performance Gap with 3D IC Technology. *IEEE Design & Test of Computers*, *22*, 556–564.

Burtscher, M., Ganusov, I., Jackson, S. J., Ke, J., Ratanaworabhan, P., & Sam, N. B. (2005). The VPC Trace-Compression Algorithms. *IEEE Transactions on Computers*, *54*, 1329–1344.

Burtscher, M., & Zorn, B. G. (2002). Hybrid Load-Value Predictors. *IEEE Transactions on Computers*, *51*, 759–774.

Burtscher, M., & Zorn, B. G. (1999). Prediction Outcome History-Based Confidence Estimation for Load Value Prediction. *Journal of Instruction-Level Parallelism*, *1*. Published. Retrieved from http://www.jilp.org/vol1/

b. Non-refereed Articles:

Rocki, K., & Burtscher, M. (2014). The Future of Accelerator Programming. *HPC Wire*. Published. Retrieved from http://www.hpcwire.com/2014/01/09/future-accelerator-programming/

3. Conference Proceedings:

a. Refereed Conference Proceedings:

Alabandi, G. A. H., Tesic, J., Rusnak, L. J., & Burtscher, M. (2021). Discovering and Balancing Fundamental Cycles in Large Signed Graphs.

Additional Comments: 27% acceptance rate

Maleki, S., Agarwal, U., Burtscher, M., & Pingali, K. (2021). BiPart: A Parallel and Deterministic Hypergraph Partitioner.

Additional Comments: 21% acceptance rate

Alabandi, G. A. H., Powers, E., & Burtscher, M. (2020). Increasing the Parallelism of Graph Coloring via Shortcutting (pp. 262–275).

Additional Comments: 23% acceptance rate

He, J., Burtscher, M., Manohar, R., & Pingali, K. (2019). SPRoute: A Scalable Parallel Negotiation-based Global Router (pp. 1–8).

Additional Comments: 24% acceptance rate

Taheri, S., Briggs, I., Burtscher, M., & Gopalakrishnan, G. (2019). DiffTrace: Efficient Whole-Program Trace Analysis and Diffing for Debugging (pp. 1–12).

Additional Comments: 28% acceptance rate

Jaiganesh, J., & Burtscher, M. (2018). A High-Performance Connected Components Implementation for GPUs (pp. 92–104).

Additional Comments: 20% acceptance rate

Maleki, S., & Burtscher, M. (2018). Automatic Hierarchical Parallelization of Linear Recurrences (pp. 128–138).

Additional Comments: 18% acceptance rate

Claggett, S., Azimi, S., & Burtscher, M. (2018). SPDP: An Automatically Synthesized Lossless Compression Algorithm for Floating-Point Data (pp. 335–344).

Burtscher, M., Hesaaraki, F., Mukka, H., & Yang, A. (2016). Real-Time Synthesis of Compression Algorithms for Scientific Data (pp. 264–275).
Additional Comments: 18% acceptance rate

Coplin, J., Yang, A., Poppe, A., & Burtscher, M. (2016). Increasing Telemetry Throughput Using Customized and Adaptive Data Compression.

Maleki, S., Yang, A., & Burtscher, M. (2016). Higher-Order and Tuple-Based Massively-Parallel Prefix Sums (pp. 539–552).
Additional Comments: 16% acceptance rate

Yang, A., Mukka, H., Hesaaraki, F., & Burtscher, M. (2015). MPC: A Massively Parallel Compression Algorithm for Scientific Data.
Additional Comments: 24% acceptance rate

Rahman, S., Burtscher, M., Zong, Z., & Qasem, A. (2015). Maximizing Hardware Prefetch Effectiveness with Machine Learning.
Additional Comments: 24% acceptance rate

Dzhagaryan, A., Milenković, A., & Burtscher, M. (2015). Quantifying Benefits of Lossless Compression Utilities on Modern Smartphones.
Additional Comments: (25% acceptance rate) [best paper candidate]

Taheri, S., Qasem, A., & Burtscher, M. (2015). A Tool for Automatically Suggesting Source-Code Optimizations for Complex GPU Kernels.
Additional Comments: 28% acceptance rate

Burtscher, M., Peng, W., Qasem, A., Shi, H., Tamir, D., & Thiry, H. (2015). A Module-based Approach to Adopting the 2013 ACM Curricular Recommendations on Parallel Computing.
Additional Comments: (36% acceptance rate)

O'Neil, M. A., & Burtscher, M. (2014). Microarchitectural Performance Characterization of Irregular GPU Kernels.

Additional Comments: (28% acceptance rate)

Ge, R., Feng, X., Burtscher, M., & Zong, Z. (2014). PEACH: Performance and Energy Aware Cooperative Hybrid Computing.
Additional Comments: 31% acceptance rate

Rabeti, H., & Burtscher, M. (2014). Feature Selection by Tree Search of Correlation-Adjusted Class Distances.

Rocki, K., Burtscher, M., & Suda, R. (2014). The Future of Accelerator Programming: Abstraction, Performance or Can We Have Both? (pp. 886–893).
Additional Comments: 15% acceptance rate

Zecena, I., Burtscher, M., Jin, T., & Zong, Z. (2013). Evaluating the Performance and Energy Efficiency of N-Body Codes on Multi-Core CPUs and GPUs (pp. 1–8).
Additional Comments: 28% acceptance rate

Milenkovic, A., Dzhagaryan, A., & Burtscher, M. (2013). Performance and Energy Consumption of Lossless Compression/Decompression Utilities on Mobile Computing Platforms (pp. 254–263).
Additional Comments: 27% acceptance rate

Burtscher, M., & Rabeti, H. (2013). GPU Acceleration of a Genetic Algorithm for the Synthesis of FSM-based Bimodal Predictors.
Additional Comments: 28% acceptance rate

Burtscher, M., & Rabeti, H. (2013). A Scalable Heterogeneous Parallelization Framework for Iterative Local Searches (pp. 1289–1298).
Additional Comments: 21% acceptance rate

Nasre, R., Burtscher, M., & Pingali, K. (2013). Data-driven versus Topology-driven Irregular Computations on GPUs (pp. 463–474).
Additional Comments: 21% acceptance rate

Nasre, R., Burtscher, M., & Pingali, K. (2013). Morph Algorithms on GPUs (pp. 147–156).
Additional Comments: (18% acceptance rate) [rated one of best papers]

Burtscher, M., Nasre, R., & Pingali, K. (2012). A Quantitative Study of Irregular Programs on GPUs (pp. 141–151).
Additional Comments: (38% acceptance rate)

Szczyrba, I., Burtscher, M., & Szczyrba, R. (2012). Validating Critical Limits of the Universal Brain Injury Criterion (pp. 199–205).
Additional Comments: (27% acceptance rate)

Ratanaworabhan, P., Burtscher, M., Kirovski, D., & Zorn, B. (2012). Hardware Support for Enforcing Isolation in Lock-Based Parallel Programs (pp. 301–310).
Additional Comments: (22% acceptance rate)

Mendez-Lojo, M., Burtscher, M., & Pingali, K. (2012). A GPU Implementation of Inclusion-based Points-to Analysis (pp. 107–116).
Additional Comments: 15% acceptance rate

Sopeju, O. A., Burtscher, M., Rane, A., & Browne, J. (2011). "AutoSCOPE: Automatic Suggestions for Code Optimizations Using PerfExpert." (pp. 19–25).
Additional Comments: 23% acceptance rate

Szczyrba, I., Burtscher, M., & Szczyrba, R. (2011). "Computer Modeling of Diffuse Axonal Injury Mechanisms." (pp. 401–407).
Additional Comments: 24% acceptance rate

O'Neil, M. A., Tamir, D., & Burtscher, M. (2011). A Parallel GPU Version of the Traveling Salesman Problem.
Additional Comments: 23% acceptance rate

Pingali, K., Nguyen, D., Kulkarni, M., Burtscher, M., Hassaan, M. A., Kaleem, R., … Sui, X. (2011). The Tao of Parallelism in Algorithms (pp. 12–25).
Additional Comments: 23% acceptance rate

Diamond, J., Burtscher, M., McCalpin, J., Kim, B.-D., Kecker, S., & Browne, J. (2011). Evaluation and Optimization of Multicore Performance Bottlenecks in Supercomputing Applications (pp. 32–43).
Additional Comments: 38% acceptance rate) [best paper award]

Hassaan, A., Burtscher, M., & Pingali, K. (2011). Ordered vs. Unordered: a Comparison of Parallelism and Work-efficiency in Irregular Algorithms (pp. 3–12).
Additional Comments: 16% acceptance rate

Burtscher, M., Kim, B.-D., Diamond, J., McCalpin, J., Koesterke, L., & Browne, J. (2010). PerfExpert: An Easy-to-Use Performance Diagnosis Tool for HPC Applications (pp. 1–11).
Additional Comments: 20% acceptance rate

Uzelac, V., Milenkovic, A., Burtscher, M., & Milenkovic, M. (2010). Real-time Unobtrusive Program Execution Trace Compression Using Branch Predictor Events (pp. 97–106).
Additional Comments: 38% acceptance rate

Burtscher, M., Livshits, B., Sinha, G., & Zorn, B. (2010). JSZap: Compressing JavaScript Code.
Additional Comments: 54% acceptance rate

Burtscher, M., & Ratanaworabhan, P. (2010). gFPC: A Self-Tuning Compression Algorithm.

Mendez-Lojo, M., Nguyen, D., Prountzos, D., Sui, X., Hassaan, M. A., Kulkarni, M., … Pingali, K. (2010). Structure-driven Optimizations for Amorphous Data-parallel Programs (pp. 3–14).
Additional Comments: (17% acceptance rate) [best paper candidate]

Uzelac, V., Milenkovic, A., Milenkovic, M., & Burtscher, M. (2009). Real-time, Unobtrusive, and Efficient Program Execution Tracing with Stream Caches and Last Stream Predictors (pp. 173–178).
Additional Comments: 35% acceptance rate

Diamond, J., Kim, B.-D., Burtscher, M., Keckler, S., Pingali, K., & Browne, J. (2009). Multicore Optimization for Ranger.
Additional Comments: 62% acceptance rate

Kulkarni, M., Burtscher, M., Cascaval, C., & Pingali, K. (2009). Lonestar: A Suite of Parallel Irregular Programs (pp. 65–76).
Additional Comments: 28% acceptance rate

Burtscher, M., & Ratanaworabhan, P. (2009). pFPC: A Parallel Compressor for Floating-Point Data (pp. 43–52).

Ratanaworabhan, P., Burtscher, M., Kirovski, D., Nagpal, R., Pattabiraman, K., & Zorn, B. (2009). Detecting and Tolerating Asymmetric Races (pp. 173–184).
Additional Comments: 24% acceptance rate

Kulkarni, M., Burtscher, M., Inkulu, R., Cascaval, C., & Pingali, K. (2009). How Much Parallelism is There in Irregular Applications? (pp. 3–14).
Additional Comments: 24% acceptance rate

Szczyrba, I., Burtscher, M., & Szczyrba, R. (2008). On the Role of a Nonlinear Stress-Strain Relation in Brain Trauma (pp. 265–271). CSREA Press.
Additional Comments: 27% acceptance rate

Ratanaworabhan, P., & Burtscher, M. (2008). Program Phase Detection based on Critical Basic Block Transitions (pp. 11–21).
Additional Comments: 35% acceptance rate

Szczyrba, I., Burtscher, M., & Szczyrba, R. (2007). A Proposed New Brain Injury Tolerance Criterion Based on the Exchange of Energy between the Skull and the Brain.
Additional Comments: 45% acceptance rate

Szczyrba, I., Burtscher, M., & Szczyrba, R. (2007). Computational Modeling of Brain Dynamics during Repetitive Head Motions (pp. 143–149). CSREA Press.

Additional Comments: 28% acceptance rate

Milenkovic, M., Milenkovic, A., & Burtscher, M. (2007). Algorithms and Hardware Structures for Unobtrusive Real-Time Compression of Instruction and Data Address Traces (pp. 283–292).

Burtscher, M., & Ratanaworabhan, P. (2007). High Throughput Compression of Double-Precision Floating-Point Data (pp. 293–302).

Ratanaworabhan, P., & Burtscher, M. (2006). Load Instruction Characterization and Acceleration of the BioPerf Programs (pp. 71–79).
Additional Comments: 32% acceptance rate

Ganusov, I., & Burtscher, M. (2006). Efficient Emulation of Hardware Prefetchers via Event-Driven Helper Threading (pp. 144–153).
Additional Comments: 26% acceptance rate

Burtscher, M., & Szczyrba, I. (2006). Computational Simulation and Visualization of Traumatic Brain Injuries (pp. 101–107).
Additional Comments: 31% acceptance rate

Ratanaworabhan, P., Ke, J., & Burtscher, M. (2006). Fast Lossless Compression of Scientific Floating-Point Data (pp. 133–142).

Ganusov, I., & Burtscher, M. (2005). Future Execution: A Hardware Prefetching Technique for Chip Multiprocessors (pp. 350–360).
Additional Comments: 25% acceptance rate

Ke, J., Burtscher, M., & Speight, E. (2005). Tolerating Message Latency through the Early Release of Blocked Receives (pp. 19–29).
Additional Comments: 31% acceptance rate

Burtscher, M., & Szczyrba, I. (2005). Numerical Modeling of Brain Dynamics in Traumatic Situations - Impulsive Translations (pp. 205–211). CSREA Press.
Additional Comments: 35% acceptance rate

Burtscher, M., & Szczyrba, I. (2005). On the Role of the Brain's Geometry in Closed Head Injuries.
Additional Comments: 49% acceptance rate

Ke, J., Burtscher, M., & Speight, E. (2005). Reducing Communication Time through Message Prefetching (pp. 557–563). CSREA Press.
Additional Comments: 28% acceptance rate

Sam, N. B., & Burtscher, M. (2005). On the Energy-Efficiency of Speculative Hardware (pp. 361–370). ACM Press.
Additional Comments: 41% acceptance rate

Burtscher, M., & Sam, N. B. (2005). Automatic Generation of High-Performance Trace Compressors (pp. 229–240). IEEE Computer Society.
Additional Comments: 34% acceptance rate

Burtscher, M., & Ganusov, I. (2004). Automatic Synthesis of High-Speed Processor Simulators (pp. 55–66).
Additional Comments: 18% acceptance rate

Ke, J., Burtscher, M., & Speight, E. (2004). Runtime Compression of MPI Messages to Improve the Performance and Scalability of Parallel Applications (pp. 59–65).
Additional Comments: 31% acceptance rate

Burtscher, M. (2004). VPC3: A Fast and Effective Trace-Compression Algorithm (pp. 167–176).
Additional Comments: 12% acceptance rate, the only single-author paper accepted

Burtscher, M., & Jeeradit, M. (2003). Compressing Extended Program Traces Using Value Predictors (pp. 159–169).
Additional Comments: 17% acceptance rate

Szczyrba, I., & Burtscher, M. (2003). On the Role of Ventricles in Diffuse Axonal Injuries (pp. 147–148).

Speight, E., & Burtscher, M. (2002). Delphi: Prediction-Based Page Prefetching to Improve the Performance of Shared Virtual Memory Systems (pp. 49–55).
Additional Comments: 32% acceptance rate

Burtscher, M., Diwan, A., & Hauswirth, M. (2002). Static Load Classification for Improving the Value Predictability of Data-Cache Misses (pp. 222–233).
Additional Comments: 17% acceptance rate

Burtscher, M., & Zorn, B. G. (2000). Hybridizing and Coalescing Load Value Predictors (pp. 81–92).
Additional Comments: 38% acceptance rate

Burtscher, M., & Zorn, B. G. (1999). Exploring Last n Value Prediction (pp. 66–76).
Additional Comments: 31% acceptance rate

4. Abstracts:

He, J., Burtscher, M., Manohar, R., & Pingali, K. (2019). SPRoute: A Scalable Parallel Negotiation-based Global Router. Published.

Rocki, K., Burtscher, M., & Suda, R. (2013). The Future of Accelerator Programming: Abstraction, Performance or Can We Have Both?, 442–443.

Burtscher, M., Peng, W., Qasem, A., Shi, H., & Tamir, D. (2013). Preparing Computer Science Students for an Increasingly Parallel World: Teaching Parallel Computing Early and Often. Published.

Dzhagaryan, A., Milenkovic, A., & Burtscher, M. (2013). Energy Efficiency of Lossless Data Compression on a Mobile Device: An Experimental Evaluation. Published.

Burtscher, M., Peng, W., Qasem, A., Shi, H., & Tamir, D. (2013). Preparing Computer Science Students for the Multicore Era: Teaching Parallel Computing in the Undergraduate Curriculum. Published.

Hassaan, A., Burtscher, M., & Pingali, K. (2010). Less is More: Trading off Work-efficiency for Scalability in Irregular Programs, 539–540.

Burtscher, M., & Zorn, B. (1999). Explaining and Exploiting Predictable Load Values. Published.

10. Other Works in Print:

Software:

Alabandi, G. A. H., & Burtscher, M. (2021). graphB+: A Scalable Balancing Algorithm for Signed Social Network Graphs. Retrieved from http://cs.txstate.edu/~burtscher/research/graphB/

Additional Comments: received all three SC'21 Artifact Evaluation Committee's badges

Burtscher, M., Kothari, A., & Fallin, W. A. (2021). SFP: A Fast Rectilinear Steiner Minimum Tree (RSMT) Heuristic. Retrieved from http://cs.txstate.edu/~burtscher/research/SFP/

Alabandi, G. A. H., Powers, E., & Burtscher, M. (2020). ECL-GC: A Fast Graph-Coloring Algorithm with Shortcutting for GPUs. Retrieved from http://cs.txstate.edu/~burtscher/research/ECL-GC/

Additional Comments: received PPoPP'20 Artifact Evaluation Committee's badge stating that the code is functional

Burtscher, M., & Pingali, K. (2018). An Efficient CUDA Implementation of the Tree-based Barnes Hut n-Body Algorithm. Retrieved from http://cs.txstate.edu/~burtscher/research/ECL-BH/

Additional Comments: 2010, 2011, 2012, 2018

Maleki, S., & Burtscher, M. (2018). PLR: An Automatic Parallelizer and Code Generator for Linear Recurrences. Retrieved from http://cs.txstate.edu/~burtscher/research/PLR/

Jaiganesh, J., & Burtscher, M. (2017). ECL-CC: A Fast Connected-Components Algorithm for GPUs. Retrieved from http://cs.txstate.edu/~burtscher/research/ECL-MIS/

Burtscher, M., & Devale, S. (2017). ECL-MIS: A Fast and High-Quality MIS Algorithm for GPUs. Retrieved from http://cs.txstate.edu/~burtscher/research/ECL-MIS/

Burtscher, M. (2016). FPcrush Real-Time Floating-Point Compressor Generator. Retrieved from http://cs.txstate.edu/~burtscher/research/FPcrush/

Maleki, S., Yang, A., & Burtscher, M. (2016). SAM: A GPU Prefix-Scan Template that Supports Higher Orders and Tuple Values. Retrieved from http://cs.txstate.edu/~burtscher/research/SAM/

Additional Comments: Received PLDI'16 Artifact Evaluation Committee's seal stating that it meets or exceeds expectations

Burtscher, M. (2016). Scientific IEEE 754 32-Bit Single-Precision Floating-Point Datasets. Retrieved from http://cs.txstate.edu/~burtscher/research/datasets/FPsingle/

Claggett, S., & Burtscher, M. (2016). SPDP: A Compression Algorithm for Single- and Double-Precision Floating-Point Data. Retrieved from http://cs.txstate.edu/~burtscher/research/SPDPcompressor/

Yang, A., & Burtscher, M. (2015). MPC: a GPU-accelerated compressor/decompressor for single- and double-precision floating-point data. Retrieved from http://cs.txstate.edu/~burtscher/research/MPC/

Claggett, S., & Burtscher, M. (2015). SPDP: A Compression Filter for HDF5. Retrieved from http://cs.txstate.edu/~burtscher/research/SPDP/

Burtscher, M. (2014). K20Power: Automatic Correction of the Power Profile from K20 and K40 Compute GPUs. Retrieved from http://www.cs.txstate.edu/~burtscher/research/K20power/

Burtscher, M. (2014). TSP_GPU2: A Fast GPU-based Solver for Large TSP Problems. Retrieved from http://www.cs.txstate.edu/~burtscher/research/TSP_GPU/

Burtscher, M., & Rabeti, H. (2013). A Scalable Heterogeneous Parallelization Framework for Iterative Local Searches. Retrieved from http://www.cs.txstate.edu/~burtscher/research/ILCS/

Nasre, R., Burtscher, M., Mendez-Lojo, M., & Pingali, K. (2013). The LonestarGPU Benchmark Suite. Retrieved from http://iss.ices.utexas.edu/?p=projects/galois/lonestargpu

Sopeju, O. A., & Burtscher, M. (2011). AutoSCOPE: Automatic Suggestions for Code Optimizations Using PerfExpert. Retrieved from http://www.cs.txstate.edu/~burtscher/research/PerfExpert/AutoSCOPE/

O'Neil, M. A., & Burtscher, M. (2011). GFC: A GPU-based Compressor for 64-Bit Floating-Point Data. Retrieved from http://www.cs.txstate.edu/~burtscher/research/GFC/

Burtscher, M., Kim, B.-D., Diamond, J., McCalpin, J., Koesterke, L., & Browne, J. (2011). PerfExpert: An Automated HPC Performance Measurement and Analysis Tool with Optimization Recommendations. Retrieved from http://www.tacc.utexas.edu/perfexpert/
Additional Comments: 2010, 2011

O'Neil, M. A., & Burtscher, M. (2011). TSP_GPU: A Fast GPU-based Solver for the Traveling Salesman Problem. Retrieved from http://www.cs.txstate.edu/~burtscher/research/TSP_GPU/

Arora, M., Burtscher, M., Deo, M., Hassaan, A., Kaleem, R., Kulkarni, M., … Sui, X. (2010). Galois: A System to Automatically Parallelize Irregular Programs at Runtime. Retrieved from http://iss.ices.utexas.edu/galois/

Livshits, B., Zorn, B., Burtscher, M., & Sinha, G. (2010). JSZap: Compressing JavaScript Source Code. Retrieved from http://research.microsoft.com/en-us/projects/jszap/

Burtscher, M., & Ratanaworabhan, P. (2009). gFPC: A Self-Tuning Compression Algorithm. Retrieved from http://users.ices.utexas.edu/~burtscher/research/gFPC/

Burtscher, M., Hassaan, A., Kulkarni, M., Mathews, A., Mendez-Lojo, M., Nguyen, D., … Sui, X. (2009). ParaMeter: A Tool to Measure the Amorphous Data Parallelism of Programs. Retrieved from http://iss.ices.utexas.edu/parameter/

Burtscher, M., & Ratanaworabhan, P. (2009). pFPC: A Parallel Compressor for 64-Bit Floating-Point Data. Retrieved from http://users.ices.utexas.edu/~burtscher/research/pFPC/

Ratanaworabhan, P., & Burtscher, M. (2008). A Miss-Triggered Program Phase Detector based on Critical Basic Block Transitions. Retrieved from http://www.csl.cornell.edu/~paruj/cbbt.html

Burtscher, M. (2008). CSC: A C-Subset to 3-Address-Code Compiler for Teaching Optimizing Compiler Courses.

Burtscher, M., & Ke, J. (2008). Scientific IEEE 754 64-Bit Double-Precision Floating-Point Datasets. Retrieved from http://www.csl.cornell.edu/~burtscher/research/FPC/datasets.html

Burtscher, M., Carribault, P., Cascaval, C., Kulkarni, M., Pingali, K., & Praun, C. von. (2008). The Lonestar Benchmark Suite. Retrieved from http://iss.ices.utexas.edu/lonestar/

Szczyrba, I., Burtscher, M., & Szczyrba, R. (2008). Traumatic Brain Injury Simulations. Retrieved from http://www.funiosoft.com/brain/

Burtscher, M., & Ratanaworabhan, P. (2006). FPC: A Lossless High-Throughput Compression Algorithm for 64-Bit Floating-Point Data. Retrieved from http://www.csl.cornell.edu/~burtscher/research/FPC/

Ratanaworabhan, P., & Burtscher, M. (2006). Load-Optimized Source Code of the BioPerf Benchmark Suite. Retrieved from http://www.bioperf.org/RB06-BioPerf-source.tar.bz2

Burtscher, M., & Sam, N. B. (2005). TCgen: A Flexible Tool to Automatically Generate Effective Trace Compressors out of User-Provided Trace Format Specifications. Retrieved from http://www.csl.cornell.edu/~burtscher/research/TCgen/

Burtscher, M., Sam, N. B., Ganusov, I., Jackson, S. J., Ratanaworabhan, P., & Ke, J. (2004). VPC3: A High-Performance Trace Compression Algorithm. Retrieved from http://www.csl.cornell.edu/~burtscher/research/tracecompression/

Hoy, J., Burtscher, M., & Gehrke, J. (2002). A Data Miner to Find Frequent Sequential Patterns. Retrieved from http://www.csl.cornell.edu/~burtscher/research/patternmining/

Jeeradit, M., & Burtscher, M. (2002). A Value Predictor Based Compression Algorithm for Program Traces. Retrieved from http://www.csl.cornell.edu/~burtscher/research/tracefilecompression/

Workshop Proceedings:

Burtscher, M. (2018). Computing a Movie of Zooming into a Fractal. In *Workshop on Education for High-Performance Computing*.

Additional Comments: 38% acceptance rate

Lu, Y.-S., Ataei, S., He, J., Hua, W., Maleki, S., Yang, Y., … Manohar, R. (2018). Parallel Tools for Asynchronous VLSI Systems. In *Workshop on Open-Source EDA Technology*.

Taheri, S., Devale, S., Gopalakrishnan, G., & Burtscher, M. (2018). ParLoT: Efficient Whole-Program Call Tracing for HPC Applications. In *Seventh Workshop on Extreme-Scale Programming Tools*.

Coplin, J., & Burtscher, M. (2016). Energy, Power, and Performance Characterization of GPGPU Benchmark Programs. In *Twelfth Workshop on High-Performance, Power-Aware Computing*.
Additional Comments: 55% acceptance rate

Goodarzi, B., Burtscher, M., & Goswami, D. (2016). Parallel Graph Partitioning on a CPU-GPU Architecture. In *Twenty Fifth International Heterogeneity in Computing Workshop*.

Coplin, J., & Burtscher, M. (2015). Effects of Source-Code Optimizations on GPU Performance and Energy Consumption. In *Eighth Workshop on General Purpose Processing Using GPUs*.
Additional Comments: 65% acceptance rate

O'Neil, M. A., & Burtscher, M. (2015). Rethinking the Parallelization of Random-Restart Hill Climbing. In *Eighth Workshop on General Purpose Processing Using GPUs*.
Additional Comments: 65% acceptance rate

Coplin, J., & Burtscher, M. (2014). Power Characteristics of Irregular GPGPU Programs. In *2014 International Workshop on Green Programming, Computing, and Data Processing*.

Li, B., Lu, Y., Li, C., Godil, A., Schreck, T., Aono, M., … Zou, C. (2014). SHREC'14 Track: Extended Large Scale Sketch-Based 3D Shape Retrieval. In *Eurographics Workshop on 3D Object Retrieval*.

Burtscher, M., Zecena, I., & Zong, Z. (2014). Measuring GPU Power with the K20 Built-in Sensor. In *Seventh Workshop on General Purpose Processing Using GPUs* (pp. 28–36).
Additional Comments: 44% acceptance rate

Burtscher, M., Shi, H., Peng, W., Tamir, D., Qasem, A., & Thiry, H. (2013). Integrating Parallel Computing into the Undergraduate Curriculum at Texas State University: Experiences from the First Year. In *Workshop on Parallel, Distributed, and High-Performance Computing in Undergraduate Curricula*.
Additional Comments: 62% acceptance rate

Ge, R., Vogt, R., Majumder, J., Alam, A., Burtscher, M., & Zong, Z. (2013). Effects of Dynamic Voltage and Frequency Scaling on a K20 GPU. In *2nd International Workshop on Power-aware Algorithms, Systems, and Architectures* (pp. 826–833).

Nasre, R., Burtscher, M., & Pingali, K. (2013). Atomic-free Irregular Computations on GPUs. In *Sixth Workshop on General Purpose Processing Using GPUs* (pp. 96–107).
Additional Comments: 39% acceptance rate

O'Neil, M. A., & Burtscher, M. (2011). Floating-Point Data Compression at 75 Gb/s on a GPU. In *Fourth Workshop on General Purpose Processing Using GPUs* (pp. 7:1–7:7).
Additional Comments: 37% acceptance rate

Sui, X., Nguyen, D., Burtscher, M., & Pingali, K. (2010). Parallel Graph Partitioning on Multicore Architectures. In *the Languages and Compilers for Parallel Computing 23rd Annual Workshop* (pp. 240–260).
Additional Comments: 38% acceptance rate

Burtscher, M., Kulkarni, M., Prountzos, D., & Pingali, K. (2008). On the Scalability of an Automatically Parallelized Irregular Application. In *Languages and Compilers for Parallel Computing 21st Annual Workshop*. Springer Verlag.
Additional Comments: 51% acceptance rate

Jackson, S. J., & Burtscher, M. (2006). Self Optimizing Finite State Machines for Confidence Estimators. In *2006 Workshop on Introspective Architecture*.
Additional Comments: 58% acceptance rate

Liu, C. C., Ganusov, I., Burtscher, M., & Tiwari, S. (2005). Improving Microprocessor Performance through 3D IC Technology. In *Semiconductor Research Corporation's TECHCON 2005 Conference*.
Additional Comments: 66% acceptance rate

Sam, N. B., & Burtscher, M. (2005). Complex Load-Value Predictors: Why We Need Not Bother. In *Fourth Annual Workshop on Duplicating, Deconstructing, and Debunking* (pp. 16–24).
Additional Comments: 70% acceptance rate

Ganusov, I., & Burtscher, M. (2005). On the Importance of Optimizing the Configuration of Stream Prefetchers. In *3rd Annual ACM SIGPLAN Workshop on Memory Systems Performance* (pp. 54–61).
Additional Comments: 33% acceptance rate

Sam, N. B., & Burtscher, M. (2004). Exploiting Type Information in Load-Value Predictors. In *Second Value-Prediction and Value-Based Optimization Workshop* (pp. 32–39).
Additional Comments: 67% acceptance rate

Burtscher, M., & Zorn, B. G. (1998). Profile-Supported Confidence Estimation for Load-Value Prediction. In *PACT'98 Workshop on Profile and Feedback-Directed Compilation*.
Additional Comments: 60% acceptance rate

B. Works Not in Print:

1. Papers Presented at Professional Meetings:

Burtscher, M., GPU Technology Conference, "A High-Quality and Fast Maximal Independent Set Algorithm for GPUs," San Jose, CA. (May 2017).

Burtscher, M., International Conference for High-Performance Computing, Networking, Storage and Analysis, "Real-Time Synthesis of Compression Algorithms for Scientific Data," Salt Lake City, UT. (November 2016).

Burtscher, M., GPU Technology Conference, "Synthesizing Effective Data Compression Algorithms for GPUs," San Jose, CA. (March 2015).

Burtscher, M., GPU Technology Conference, "A High-Speed 2-Opt TSP Solver for Large Problem Sizes," San Jose, CA. (March 2014).

Burtscher, M., GPU Technology Conference, "Measuring GPU Power with the K20 Built-in Sensor," San Jose, CA. (March 2014).

Burtscher, M., "Workshop on General-Purpose Processing Using GPUs," Salt Lake City, UT. (March 2014).

Burtscher, M., 27th IEEE International Parallel & Distributed Processing Symposium, "A Scalable Heterogeneous Parallelization Framework for Iterative Local Searches," Boston, MA. (May 2013).

Burtscher, M., GPU Technology Conference, "Implementing and Tuning Irregular Programs on GPUs," San Jose, CA. (March 2013).

Burtscher, M., GPU Technology Conference, "An Efficient GPU Implementation of the Irregular Barnes-Hut N-Body Algorithm," San Jose, CA. (May 2012).

Burtscher, M., International Conference on Parallel and Distributed Processing Techniques and Applications, "A Parallel GPU Version of the Traveling Salesman Problem," Las Vegas, NV. (July 2011).

Burtscher, M., International Conference on Parallel and Distributed Processing Techniques and Applications, "AutoSCOPE: Automatic Suggestions for Code Optimizations Using PerfExpert," Las Vegas, NV. (July 2011).

Burtscher, M., SC 2010 International Conference for High-Performance Computing, Networking, Storage and Analysis, "PerfExpert: An Easy-to-Use Performance Diagnosis Tool for HPC Applications," New Orleans, LA. (November 2010).

Burtscher, M., 2010 Data Compression Conference, "gFPC: A Self-Tuning Compression Algorithm," Snowbird, UT. (March 2010).

Burtscher, M., "pFPC: A Parallel Compressor for Floating-Point Data," 2009 Data Compression Conference, Snowbird, UT. (March 2009).

Burtscher, M., Languages and Compilers for Parallel Computing 21st Annual Workshop, "On the Scalability of an Automatically Parallelized Irregular Application," Edmonton, Canada. (July 2008).

Burtscher, M., Data Compression Conference, "High Throughput Compression of Double-Precision Floating-Point Data," Snowbird, UT. (March 2007).

Burtscher, M., International Symposium on Code Generation and Optimization, "Automatic Generation of High-Performance Trace Compressors," San Jose, CA. (March 2005).

Burtscher, M., 37th Annual IEEE/ACM International Symposium on Microarchitecture, "Automatic Synthesis of High-Speed Processor Simulators," Portland, OR. (December 2004).

Burtscher, M., Joint International Conference on Measurement and Modeling of Computer Systems, "VPC3: A Fast and Effective Trace-Compression Algorithm," New York, NY. (June 2004).

Burtscher, M., International Conference on Parallel Architectures and Compilation Techniques, "Compressing Extended Program Traces using Value Predictors," New Orleans, LA. (September 2003).

Burtscher, M., International Conference on Computer Design, "Hybridizing and Coalescing Load Value Predictors," Austin, TX. (September 2000).

Burtscher, M., International Conference on Parallel Architectures and Compilation Techniques, "Exploring Last n Value Prediction," Newport Beach, CA. (October 1999).

Burtscher, M., PACT'98 Workshop on Profile and Feedback-Directed Compilation, "Profile-Supported Confidence Estimation for Load-Value-Prediction," Paris, France. (October 1998).

2. Invited Talks, Lectures, and Presentations:

Burtscher, M., "Automatic Generation of Algorithms for High-Speed Reliable Lossy Compression," DOE Data Reduction for Science kickoff meeting, virtual. (December 2021).

Burtscher, M., "Scientific Research in the Efficient Computing Laboratory," Texas State University, Department of Computer Science, San Marcos, TX. (September 2021).

Burtscher, M., "Irregular Sweeps on GPUs," University of Texas at Austin, PSAAP III first-year review, virtual. (August 2021).

Burtscher, M., GPU Technology Conference, "High-Speed Graph Coloring on GPUs," virtual. (April 2021).

Burtscher, M., "Increasing the Parallelism of Graph Coloring via Shortcutting," University of Texas at Austin, PSAAP III group, virtual. (December 2020).

Burtscher, M., "Scientific Research in the Efficient Computing Laboratory," Texas State University, Department of Computer Science, San Marcos, TX. (September 2020).

Burtscher, M., "Scientific Research in the Efficient Computing Laboratory," Texas State University, Department of Computer Science, San Marcos, TX. (September 2019).

Burtscher, M., "A High-Quality and Fast Maximal Independent Set Algorithm for GPUs," ETH Zurich, Department of Computer Science, Zurich, Switzerland. (June 2019).

Burtscher, M., "GPU Hardware and CUDA Programming," University of Texas at Austin, Department of Computer Science, Austin, TX. (May 2019).

Burtscher, M., "High-Performance Design and Implementation of Complex Algorithms for GPUs," AMD, Austin, TX. (April 2019).

Burtscher, M., Workshop on Education for High-Performance Computing, "Computing a Movie of Zooming into a Fractal," Dallas, TX. (November 2018).

Burtscher, M., "Scientific Research in the Efficient Computing Laboratory," Texas State University, Department of Computer Science, San Marcos, TX. (September 2018).

Burtscher, M., "Automatic Hierarchical Parallelization of Linear Recurrences," ETH Zurich, Department of Computer Science, Zurich, Switzerland. (July 2018).

Burtscher, M., "A High-Performance Connected Components Implementation for GPUs," The University of Texas at Austin, Department of Computer Science, Austin, TX. (June 2018).

Burtscher, M., International Symposium on High-Performance Parallel and Distributed Computing, "A High-Performance Connected Components Implementation for GPUs," Tempe, AZ. (June 2018).

Burtscher, M., "Automatic Hierarchical Parallelization of Linear Recurrences," Oakland University, Department of Electrical and Computer Engineering, Auburn Hills, MI. (April 2018).

Burtscher, M., "Automatic Hierarchical Parallelization of Linear Recurrences," Texas A&M University, Department of Computer Science and Engineering, College Station, TX. (April 2018).

Burtscher, M., GPU Technology Conference, "Automatic Hierarchical Parallelization of Linear Recurrences," San Jose, CA. (March 2018).

Burtscher, M., Data Compression Conference, "SPDP: An Automatically Synthesized Lossless Compression Algorithm for Floating-Point Data," Snowbird, UT. (March 2018).

Burtscher, M., "Scientific Research in the Efficient Computing Laboratory," Texas State University, Department of Computer Science, San Marcos, TX. (September 2017).

Burtscher, M., "A High-Quality and Fast Maximal Independent Set Algorithm for GPUs," University of Texas at Austin, Department of Computer Science, Austin, TX. (May 2017).

Burtscher, M., "Synthesizing Effective Compression Algorithms for CPUs, GPUs, and Space Probes," The University of Utah, Department of Computer Science, Salt Lake City, UT. (November 2016).

Burtscher, M., "An Efficient GPU Implementation of the Irregular Barnes-Hut N-Body Algorithm," The University of Texas at Austin, Department of Computer Science, Austin, TX. (October 2016).

Burtscher, M., "An Efficient GPU Implementation of the Irregular Barnes-Hut N-Body Algorithm," Southern Methodist University, Department of Mathematics, Dallas, TX. (April 2015).

Burtscher, M., Workshop on Parallel Computing in the Undergraduate Curriculum: The Early-and-Often Approach, "Introducing Parallel Computing Concepts at various Stages in the CS Curriculum," San Marcos, TX. (August 2014).

Burtscher, M., "An Efficient GPU Implementation of the Irregular Barnes-Hut N-Body Algorithm," University of Alabama in Huntsville, Department of Electrical and Computer Engineering. (April 2013).

Burtscher, M., "An Efficient GPU Implementation of the Irregular Barnes-Hut N-Body Algorithm," Marquette University, Department of Mathematics, Statistics, and Computer Science. (September 2012).

Burtscher, M., "Parallelizing and Optimizing Programs for GPU Acceleration using CUDA (tutorial)," International Conference on Parallel Architectures and Compilation Techniques, Minneapolis, MN. (September 2012).

Burtscher, M., TACC Summer Supercomputing Institute, "PerfExpert – Really Simple Program Optimization (tutorial)," Austin, TX. (August 2012).

Burtscher, M., ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming, "Parallelizing and Optimizing Programs for GPU Acceleration using CUDA (tutorial)," New Orleans, LA. (February 2012).

Burtscher, M., ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming, "PerfExpert – Really Simple Program Optimization (tutorial)," New Orleans, LA. (February 2012).

Burtscher, M., International Conference on Parallel Architectures and Compilation Techniques., "Introducing Parallel Computing Concepts at various Stages in the CS Curriculum," Galveston, TX. (October 2011).

Burtscher, M., IEEE Cluster, "PerfExpert – Really Simple Program Optimization (tutorial)," Austin, TX. (September 2011).

Burtscher, M., TACC Summer Supercomputing Institute, "PerfExpert – Really Simple Program Optimization (tutorial)," Austin, TX. (August 2011).

Burtscher, M., Workshop on GPU Programming for Scientific Applications, "Performance Optimization of CUDA Programs (two invited lectures)," University of Coimbra, Portugal. (July 2011).

Burtscher, M., Texas Advanced Computing Center, "PerfExpert – Really Simple Program Optimization (tutorial)," Austin, TX. (April 2011).

Burtscher, M., "An Efficient GPU Implementation of the Irregular Barnes-Hut N-Body Algorithm," The University of Texas at Austin, Department of Computer Science. (March 2011).

Burtscher, M., "PerfExpert: An Easy-to-Use Performance Diagnosis Tool for HPC Applications," University of Minho (Portugal), Department of Computer Science, Portugal. (January 2011).

Burtscher, M., Winter Advanced Computing Seminar, "Writing Efficient CUDA Programs (invited lecture)," University of Minho, Portugal. (January 2011).

Burtscher, M., TeraGrid 2010 Tutorial, "PerfExpert: An Automated Approach to Analyzing and Optimizing the Node-Level Performance of HPC Applications," Pittsburgh, PA. (August 2010).

Burtscher, M., "New Techniques for Exploiting GPU, Multicore, and Distributed-Memory Parallelism," Texas State University-San Marcos, Department of Computer Science. (April 2010).

Burtscher, M., Institute for Computational Engineering and Sciences, "Barnes Hut N-body Simulation on a GPU," The University of Texas at Austin. (March 2010).

Burtscher, M., "Towards a Science of Parallel Programming," University of Colorado at Boulder, Department of Computer Science. (March 2010).

Burtscher, M., "PerfExpert: a Core/Chip/Node Performance Assessment Tool for HPC Systems," Texas Advanced Computing Center, The University of Texas at Austin. (November 2009).

Burtscher, M., 16th EuroPVM/MPI Conference, "Real-Time Message Compression in Software (invited keynote)," Espoo, Finland. (September 2009).

Burtscher, M., CSC - IT Center for Science (Finnish Supercomputing Center), "Towards a Science of Parallel Programming," Espoo, Finland. (September 2009).

Burtscher, M., "Using Multiple Cores to Speed up Sequential Code," The University of Texas at San Antonio, Department of Computer Science. (March 2009).

Burtscher, M., "Using Multiple Cores to Speed up Sequential Code," The University of Texas at San Antonio, Department of Electrical and Computer Engineering. (February 2009).

Burtscher, M., SC 2008 International Conference for High-Performance Computing, Networking, Storage and Analysis; NSF High-End Computing University Research Activity (HECURA) Birds-of-a-Feather Session, "Language and System Support for Petascale Irregular Applications," Austin, TX. (November 2008).

Burtscher, M., "Accelerating Message Passing," Texas Advanced Computing Center, The University of Texas at Austin. (May 2007).

Burtscher, M., "New Approaches to Reduce the Data Access Latency in Microprocessors," University of New Mexico, Department of Computer Science. (April 2007).

Burtscher, M., "New Approaches to Reduce the Data Access Latency in Microprocessors," IBM Corporation, Austin, TX. (April 2007).

Burtscher, M., "New Approaches to Reduce the Data Access Latency in Microprocessors," The University of Texas at Austin, Department of Computer Sciences. (March 2007).

Burtscher, M., "New Approaches to Reduce the Data Access Latency in Microprocessors," Texas A&M University, Department of Electrical and Computer Engineering. (March 2007).

Burtscher, M., "Using Architecture and Code Optimization Techniques to Create Fast and Effective Data Compressors," University of California, Berkeley, Department of Electrical Engineering and Computer Sciences. (December 2006).

Burtscher, M., "Using Architecture and Code Optimization Techniques to Create Fast and Effective Data Compressors," Lawrence Livermore National Laboratory, Livermore, CA. (December 2006).

Burtscher, M., "Using Architecture and Code Optimization Techniques to Create Fast and Effective Data Compressors," Microsoft Research, Redmond, WA. (December 2006).

Burtscher, M., "Using Architecture and Code Optimization Techniques to Create Fast and Effective Data Compressors," Carnegie Mellon University, Department of Electrical and Computer Engineering. (October 2006).

Burtscher, M., "Applying Value Speculation Techniques to New Domains," Harvard University, Department of Computer Science. (November 2005).

Burtscher, M., "Applying Value Speculation Techniques to New Domains," Northeastern University, Department of Electrical and Computer Engineering. (November 2005).

Burtscher, M., "Applying Value Speculation Techniques to New Domains," Princeton University, Department of Computer Science. (November 2005).

Burtscher, M., "Applying Value Speculation Techniques to New Domains," University of California, San Diego, Department of Computer Science and Engineering. (October 2005).

Burtscher, M., "Applying Value Speculation Techniques to New Domains," University of Illinois at Urbana-Champaign, Department of Computer Science. (September 2005).

Burtscher, M., "The Development of an Effective Trace-Compression Algorithm," Cornell University, School of Electrical and Computer Engineering. (April 2005).

Burtscher, M., "The Development of an Effective Trace-Compression Algorithm," University of Wisconsin-Madison, Department of Electrical and Computer Engineering. (April 2005).

Burtscher, M., "Automatic Generation of High-Performance Trace Compressors," IBM Corporation, Austin, TX. (December 2004).

Burtscher, M., "Automatic Synthesis of High-Speed Processor Simulators," University of Colorado at Boulder, Department of Computer Science. (December 2004).

Burtscher, M., "Improving Energy-Efficiency through Load-Value Prediction," Intel Corporation, Santa Clara, CA. (May 2004).

Burtscher, M., "Improving Energy-Efficiency through Load-Value Prediction," Transmeta Corporation, Santa Clara, CA. (May 2004).

Burtscher, M., "Techniques for Improving the Predictability of Critical Loads," Intel Corporation, Santa Clara, CA. (August 2003).

Burtscher, M., "Trace Compression using Value Predictors," Microsoft Research, Redmond, WA. (June 2003).

Burtscher, M., "Trace Compression using Value Predictors," Syracuse University, Department of Electrical Engineering and Computer Science. (April 2003).

Burtscher, M., "Trace Compression using Value Predictors," Rensselaer Polytechnic Institute, Department of Computer Science. (March 2003).

Burtscher, M., "Trace Compression using Value Predictors," University of California, Riverside, Department of Computer Science and Engineering. (February 2003).

Burtscher, M., "Trace Compression using Value Predictors," Cornell University, School of Electrical and Computer Engineering. (December 2002).

Burtscher, M., "Trace Compression using Value Predictors," University of Colorado at Boulder, Department of Computer Science. (October 2002).

Burtscher, M., "Designing a Small High-Performance Load-Value Predictor," Cornell University, Department of Computer Science. (January 2002).

Burtscher, M., "Value-Prediction Research at Cornell," Cornell University, Department of Computer Science. (January 2002).

Burtscher, M., "Designing a Small High-Performance Load-Value Predictor," ETH Zurich, Department of Computer Science. (November 2001).

Burtscher, M., "Designing a Small High-Performance Load-Value Predictor," University of Rochester, Department of Electrical and Computer Engineering and Department of Computer Science. (October 2001).

Burtscher, M., "Designing a Small High-Performance Load-Value Predictor," Intel Corporation, Santa Clara, CA. (September 2001).

Burtscher, M., "Load Value Prediction (guest lecture)," Cornell University, School of Electrical and Computer Engineering. (February 2001).

Burtscher, M., "Designing a Small High-Performance Load-Value Predictor," Hewlett-Packard Company, Ft. Collins, CO. (December 2000).

Burtscher, M., "Designing a Small High-Performance Load-Value Predictor," Cornell University, School of Electrical and Computer Engineering. (November 2000).

Burtscher, M., "Designing a Small High-Performance Load-Value Predictor," Lockheed Martin Corporation, Owego, NY. (November 2000).

Burtscher, M., "Designing a Small High-Performance Load-Value Predictor," Compaq Computer Corporation, Shrewsbury, MA. (October 2000).

Burtscher, M., "Predictability and Exploitability of Load Values," Microsoft Research, Redmond, WA. (June 2000).

Burtscher, M., "Improving Context-Based Load Value Prediction (dissertation defense)," University of Colorado at Boulder, Department of Computer Science. (April 2000).

Burtscher, M., "The Evolution of a Load Value Predictor," University of Arizona, Tucson, Department of Computer Science. (April 2000).

Burtscher, M., "The Evolution of a Load Value Predictor," University of California, Santa Cruz, Department of Computer Science. (April 2000).

Burtscher, M., "The Evolution of a Load Value Predictor," North Carolina State University, Department of Electrical and Computer Engineering. (March 2000).

Burtscher, M., "The Evolution of a Load Value Predictor," Cornell University, School of Electrical Engineering. (February 2000).

Burtscher, M., "The Evolution of a Load Value Predictor," University of Massachusetts at Amherst, Department of Computer Science and Department of Electrical and Computer Engineering. (February 2000).

Burtscher, M., "The Evolution of a Load Value Predictor," Purdue University, Department of Computer Science. (February 2000).

Burtscher, M., "The Evolution of a Load Value Predictor," Oregon State University, Department of Computer Science and Department of Electrical and Computer Engineering. (February 2000).

Burtscher, M., "The Evolution of a Load Value Predictor," Colorado State University, Department of Computer Science. (January 2000).

Burtscher, M., "IA-64 Architecture and Novelties," University of Colorado at Boulder, Department of Computer Science. (November 1999).

Burtscher, M., "Designing a Coalesced-Hybrid Load Value Predictor," University of California, Santa Barbara, Department of Computer Science. (July 1999).

Burtscher, M., "Designing a Coalesced-Hybrid Load Value Predictor," University of California, Irvine, Department of Information and Computer Science. (July 1999).

Burtscher, M., Conference on Programming Language Design and Implementation, "Explaining and Exploiting Predictable Load Values (student poster session)," Atlanta, GA. (May 1999).

Burtscher, M., "Designing a Coalesced-Hybrid Load Value Predictor," Stanford University, Department of Computer Science. (March 1999).

Burtscher, M., "Designing a Coalesced-Hybrid Load Value Predictor," Hewlett-Packard Company, Cupertino, CA. (March 1999).

Burtscher, M., "Designing a Coalesced-Hybrid Load Value Predictor," Silicon Graphics, Inc, Mountain View, CA. (March 1999).

Burtscher, M., "Designing a Coalesced-Hybrid Load Value Predictor," Intel Corporation, Santa Clara, CA. (March 1999).

Burtscher, M., "Designing a Coalesced-Hybrid Load Value Predictor," Transmeta Corporation, Santa Clara, CA. (March 1999).

Burtscher, M., "Designing a Coalesced-Hybrid Load Value Predictor," Sun Microsystems, Sunnyvale, CA. (March 1999).

Burtscher, M., "Evolution of a Load Value Predictor," University of Colorado at Boulder, Department of Computer Science. (December 1998).

Burtscher, M., "Prediction Outcome History-Based Load Value Prediction," Colorado Advanced Software Institute Symposium, Denver, CO. (October 1998).

Burtscher, M., "History-Based Load Value Prediction," Hewlett-Packard Company, Cupertino, CA. (June 1998).

Burtscher, M., "Long-Latency Load Value Prediction," ETH Zurich, Department of Computer Science. (June 1998).

Burtscher, M., "Load Value Prediction Using History Bits," University of Colorado at Boulder, Department of Computer Science. (April 1998).

Burtscher, M., "Oberon: An Extensible Operating System (guest lecture)," University of Colorado at Boulder, Department of Computer Science. (March 1998).

Burtscher, M., "Next Generation Programming Language Implementation Technology (guest lecture)," University of Colorado at Boulder, Department of Computer Science. (January 1998).

Burtscher, M., "Static Branch Probability Estimation," University of Colorado at Boulder, Department of Computer Science. (April 1997).

Burtscher, M., "Dynamic Reoptimization," University of Colorado at Boulder, Department of Computer Science. (November 1996).

Burtscher, M., "Iterative Methods for Linear Equations," ETH Zurich, Department of Computer Science. (December 1994).

5. Other Works not in Print:

c. Other Works Not in Print:

Patents:

Burtscher, Martin, Devale, Sindhu. "System and Method for Identifying Maximal Independent Sets in Parallel". United States. Number / ID: United States Patent 10,599,638. (Date Awarded: 2020).

Burtscher, Martin, Ganusov, Ilya. "Future Execution Prefetching Technique and Architecture". United States. Number / ID: United States Patent 7,730,263. (Date Licensed: 2014).

D. Scholarly / Creative Fellowships, Awards, Honors:

Award / Honor Recipient: Presidential Distinction Award for Excellence in Scholarly/Creative Activity, College of Science and Engineering, Texas State University.
August 2021

Award / Honor Recipient: Supercomputing Allocation, Texas Advanced Computing Center.
January 2019 - December 2019

Additional Comments: Maverick supercomputer: 4000 SUs awarded Lonestar5 supercomputer: 5000 SUs awarded
January 2018 - December 2018

Additional Comments: Maverick supercomputer: 50000 SUs awarded Lonestar5 supercomputer: 5000 SUs awarded

Award / Honor Recipient: College Achievement Award for Excellence in Teaching, College of Science and Engineering, Texas State University.
August 2019

Award / Honor Recipient: Supercomputing Allocation, San Diego Supercomputer Center.
November 2017 - November 2018

Award / Honor Recipient: College Achievement Award for Excellence in Scholarly/Creative Activity, College of Science and Engineering, Texas State University.
August 2017
August 2014

Award / Honor Recipient: Highly-Rated Speaker badge, GPU Technology Conference.
March 2015
March 2014

Award / Honor Recipient: Distinguished Scientist, Association for Computing Machinery (ACM).
November 2014

Award / Honor Recipient: co-host a “GTC Hangout”, GPU Technology Conference.
March 2014

Award / Honor Recipient: Academic Partnership Award, NVIDIA Corporation.
November 2011

Award / Honor Recipient: Best Paper Award, IEEE International Symposium on Performance Analysis of Systems and Software.
April 2011

Award / Honor Recipient: Clive Fraser Baillie Memorial Award, Department of Computer Science, University of Colorado at Boulder.
1999
Additional Comments: Fall 1999

Fellowship Recipient: Advanced Allocation Fellowship, Department of Computer Science, University of Colorado at Boulder.
1996 - 1997

Award / Honor Recipient: Scholarship, ETH Zurich.
1990 - 1996

E. Scholarly / Creative Professional Development Activities Attended:

DOE meeting, "DOE Data Reduction for Science kickoff meeting," virtual. (December 2021).

Conference Attendance, "GPU Technology Conference," virtual. (March 2021).

Conference Attendance, "GPU Technology Conference," virtual. (March 2020).

Conference Attendance, "GPU Technology Conference," San Jose, CA. (May 2017).

Conference Attendance, "International Conference for High-Performance Computing, Networking, Storage and Analysis," Salt Lake City, UT. (November 2016).

Conference Attendance, "GPU Technology Conference," San Jose, CA. (April 2016).

IV. SERVICE

A. Institutional

2. College:

Member, Ad Hoc Presidential Awards Committee. (2018).

Additional Comments: College of Science and Engineering, Texas State University

Inaugural Academic Advisor, IEEE CS Student Chapter at Texas State University College of Science and Engineering, Texas State University. (2013 - 2017).

3. Department/School:

Chair, Presidential Awards Nomination Committee. (2018 - Present).

Member, NCWIT Extension Services Team. (2018 - Present).

Additional Comments: Department of Computer Science, Texas State University

Member, Personnel Committee. (2015 - Present).
Additional Comments: Department of Computer Science, Texas State University

Interim Chair and Member, Ph.D. Program Committee. (2012 - Present).

Additional Comments: Department of Computer Science, Texas State University

Member, Undergraduate Committee. (2011 - Present).
Additional Comments: Department of Computer Science, Texas State University 2011 - 2012, 2014 - present

Member, Procedures and Policy Committee. (2010 - Present).
Additional Comments: Department of Computer Science, Texas State University 2010 - 2014, 2015 - present

Member, Faculty Search Committee, Department of Computer Science, Texas State University. (2018 - 2021).

Additional Comments: 2018/2019 and 2020/2021

Judge, REU Poster. (July 2020).

Member, Space Committee. (2011 - 2018).

Additional Comments: Department of Computer Science, Texas State University 2011 - present

Course Coordinator, Computer Architecture. (2014 - 2017).

Additional Comments: Department of Computer Science, Texas State University

Chair, Faculty Search Committee, Department of Computer Science, Texas State University. (2015 - 2016).

Member, General Recruiting Committee Member. (2005 - 2006).
Additional Comments: School of Electrical and Computer Engineering, Cornell University

Member, Computer Advisory Committee Member. (2002 - 2005).
Additional Comments: School of Electrical and Computer Engineering, Cornell University

Advisor, Cornell ASTRO Team Advisor. (2002 - 2003).
Additional Comments: School of Electrical and Computer Engineering, Cornell University

Member, Graduate Committee Member. (2001 - 2003).
Additional Comments: School of Electrical and Computer Engineering, Cornell University

Student Representative, Graduate Committee Senior Student Representative. (1998 - 1999).
Additional Comments: Department of Computer Science, University of Colorado at Boulder

University Mentor, Mentor in the European Exchange Students Program. (1995).
Additional Comments: Department of Computer Science, ETH Zurich

B. Professional:

Faculty Mentor, Texas State University, San Marcos. (2019 - Present).

Additional Comments: Jelena Tesic

Advisory Board Member, Hyperion Core. (2015 - Present).

Member, National Center for Women & Information Technology (NCWIT). (2015 - Present).

Distinguished Member, Association for Computing Machinery (ACM). (2014 - Present).

Senior Member, Association for Computing Machinery (ACM). (2006 - Present).

Senior Member, Institute of Electrical and Electronics Engineers (IEEE). (2006 - Present).

Member, Association for Computing Machinery (ACM). (1998 - Present).

Member, IEEE Computer Society. (1997 - Present).

Member, Institute of Electrical and Electronics Engineers (IEEE). (1997 - Present).

External Review Committee Member, IEEE/ACM International Symposium on Computer Architecture. (2021 - 2022).

Additional Comments: 2021, 2022

Reviewer / Referee, Annual International Symposium on Computer Architecture. (2000 - 2022).

Additional Comments: 2000, 2001, 2002, 2003, 2007, 2021, 2022

External Review Committee Member, IEEE/ACM International Symposium on Microarchitecture. (2021).

Additional Comments: 2021

Program Committee Member, IEEE International Symposium on Performance Analysis of Systems and Software. (2021).

Additional Comments: 2021

Reviewer / Referee, ACM Transactions on Design Automation of Electronic Systems. (2021).

Additional Comments: 2021

Program Committee Member, International Workshop on Big Data Reduction. (2020 - 2021).

Additional Comments: 2020

Reviewer / Referee, International Workshop on Big Data Reduction. (2020 - 2021).

Additional Comments: 2020, 2021

Program Committee Member, International Workshop on Data Analysis and Reduction for Big Scientific Data. (2017 - 2021).

Additional Comments: 2017 (2), 2018 (2), 2019 (1), 2020, 2021

Reviewer / Referee, IEEE International Symposium on Performance Analysis of Systems and Software. (2009 - 2021).

Additional Comments: 2009, 2012, 2019, 2021

Reviewer / Referee, Data Compression Conference. (2008 - 2021).

Additional Comments: 2008, 2012, 2016, 2018, 2021

Reviewer / Referee, Annual International Symposium on Microarchitecture. (1998 - 2021).

Additional Comments: 1998, 2002, 2003, 2004, 2006, 2009, 2011, 2018, 2021

Reviewer / Referee, Engineering Science and Technology. (2020).

Additional Comments: 2020

Reviewer / Referee, Future Generation Computer Systems. (2020).

Additional Comments: 2020

Reviewer / Referee, IARCS Annual Conference on Foundations of Software Technology and Theoretical Computer Science. (2020).

Additional Comments: 2020

Reviewer / Referee, International Journal of High Performance Computing Applications. (2020).

Additional Comments: 2020

Reviewer / Referee, International Workshop on Data Reduction for Big Scientific Data. (2017 - 2020).

Additional Comments: 2017 (2), 2018, 2019, 2020

Reviewer / Referee, Journal of Parallel and Distributed Computing. (2014 - 2020).

Additional Comments: 2011, 2014, 2015, 2018, 2020

Reviewer / Referee, ACM Transactions on Architecture and Code Optimization. (2003 - 2020).

Additional Comments: 2003, 2004, 2005, 2006, 2011, 2016, 2017, 2018, 2020

Reviewer / Referee, Computer Graphics Forum. (2019).

Reviewer / Referee, National Center for Women & Information Technology. (2019).

Reviewer / Referee, Springer Verlag. (2019).

Reviewer / Referee, National Center for Women & Information Technology. (2017 - 2019).

Additional Comments: 2017, 2018, 2019 (for female high-school students)

Principal Investigator, NVIDIA GPU Education Center. (2012 - 2019).

Reviewer / Referee, IEEE Transactions on Parallel and Distributed Systems. (2012 - 2019).

Additional Comments: 2003, 2006, 2012, 2013, 2016, 2018, 2019

Reviewer / Referee, Workshop on General-Purpose Processing Using GPUs. (2012 - 2019).

Additional Comments: 2012, 2013, 2016, 2017, 2018, 2019

Reviewer / Referee, National Aeronautics and Space Administration. (2008 - 2019).

Additional Comments: 2008, 2019

Reviewer / Referee, IEEE Computer Architecture Letters. (2003 - 2019).

Additional Comments: 2003, 2006, 2015, 2017, 2018, 2019

Faculty Mentor, Oakland University PI Academy. (2018).

Additional Comments: Shadi Alawneh

Reviewer / Referee, Concurrency and Computation: Practice and Experience. (2018).

Additional Comments: 2018

Reviewer / Referee, Journal of Applied Mathematics & Information Sciences. (2018).

Additional Comments: 2018

Program Committee Member, Workshop on General-Purpose Processing Using GPUs. (2012 - 2018).

Additional Comments: 2012, 2013, 2016, 2017, 2018

Program Committee Member, ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming. (2009 - 2018).

Additional Comments: 2009, 2011 (ERC), 2013, 2014, 2015 (ERC), 2017 (ERC), 2018 (ERC)

Reviewer / Referee, ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming. (2009 - 2018).

Additional Comments: 2009, 2010, 2011, 2012, 2013, 2014, 2015, 2017, 2018

Reviewer / Referee, International Conference on Architectural Support for Programming Languages and Operating Systems. (2006 - 2018).

Additional Comments: 2006, 2009, 2010, 2018

Advisory Board Member, Accelogic. (2014 - September 2018).

Reviewer / Referee, Euro-Par. (2015 - 2017).

Additional Comments: 2015, 2017

Reviewer / Referee, ACM Transactions on Parallel Computing. (2013 - 2017).

Additional Comments: 2013, 2014, 2015, 2017

Program Committee Member, Workshop on Education for High-Performance Computing. (2016).

Additional Comments: 2016

Reviewer / Referee, ACM Computing Surveys. (2016).

Reviewer / Referee, ACM Transactions on Modeling and Computer Simulation. (2016).
Additional Comments: 2004, 2006

Reviewer / Referee, Department of Energy, Exascale Computing Project. (2016).

Reviewer / Referee, EuroMPI. (2016).

Reviewer / Referee, IEEE Transactions on Computers. (2012 - 2016).
Additional Comments: 2001, 2004

Program Committee Member, IEEE Cluster Conference. (2015).

Reviewer / Referee, IEEE Cluster Conference. (2015).

Reviewer / Referee, IET Computers & Digital Techniques. (2015).

Reviewer / Referee, International Conference on Network and Parallel Computing. (2015).

Reviewer / Referee, Synthesis Lectures on Computer Architecture. (2015).

Reviewer / Referee, ACM SIGPLAN Conference on Programming Language Design and Implementation. (2014 - 2015).
Additional Comments: 2011

Program Committee Member, ACM SIGPLAN Conference on Programming Language Design and Implementation. (2011 - 2015).
Additional Comments: 2011 (ERC), 2014, 2015 (ERC)

Chair and Host, Co-host, GTC Speakers Hangout, GPU Technology Conference. (2014).

Co-Founder and Organizer, Regional Workshop on Parallel Computing in the Undergraduate Curriculum. (2014).

Session Chair, IEEE International Parallel & Distributed Processing Symposium. (2013).

Session Chair, Workshop on General-Purpose Processing Using GPUs. (2013).

Reviewer / Referee, ACM Symposium on Parallelism in Algorithms and Architectures. (2012).

Reviewer / Referee, International Symposium on High-Performance Computer Architecture. (2012).
Additional Comments: 2003, 2004, 2006

Reviewer / Referee, Parallel and Distributed Computing and Networks. (2012).

Co-Founder and Organizer, CUDA Optimization Tutorial. (2011 - 2012).

Co-Founder and Organizer, PerfExpert Tutorial. (2010 - 2012).
Additional Comments: 2010, 2011 (3), 2012 (2)

Finance Chair, International Conference on Parallel Architectures and Compilation Techniques. (2011).

Program Committee Member, International Computer Science and Engineering Conference. (2011).

Reviewer / Referee, GPU Computing Gems. (2011).

Reviewer / Referee, International Computer Science and Engineering Conference. (2011).

Reviewer / Referee, International Conference on Computer and Communication Technology. (2011).

Workshops and Tutorials Chair, Int. Symposium on High-Performance Computer Architecture. (2011).

Co-Founder and Organizer, Parallelizing Irregular Applications through the Exploitation of Amorphous Data-Parallelism Tutorial. (2010).

Poster Chair, ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming. (2010).

Reviewer / Referee, ACM Transactions on Computer Systems. (2010).

Reviewer / Referee, International Conference on High Performance Embedded Architectures & Compilers. (2010).

Reviewer / Referee, Annual International Conference on Supercomputing. (2009 - 2010).
Additional Comments: 2002

Associate Editor, Journal of Instruction-Level Parallelism. (2005 - 2010).

Registration Chair, International Symposium on Computer Architecture. (2009).

Reviewer / Referee, IEEE International Parallel & Distributed Processing Symposium. (2009).
Additional Comments: 2002, 2003, 2006

Reviewer / Referee, Workshop on Data Management on New Hardware. (2009).

Reviewer / Referee, Workshop on Languages and Compilers for Parallel Computing. (2009).

Program Committee Member, IEEE International Symposium on Workload Characterization. (2008).

Reviewer / Referee, IEEE International Symposium on Workload Characterization. (2008).
Additional Comments: 2005

Reviewer / Referee, IEEE Micro. (2008).

Reviewer / Referee, Scientific Programming. (2008).

Session Chair, International Symposium on Performance Analysis of Systems and Software. (2008).

Reviewer / Referee, ACM Transactions on Computer Systems. (2007).

Program Committee Member, Memory Systems Performance and Correctness Workshop. (2006).

Reviewer / Referee, ACM Computing Surveys. (2006).

Reviewer / Referee, Design, Automation and Test in Europe Conference. (2006).

Reviewer / Referee, Memory Systems Performance and Correctness Workshop. (2006).

Reviewer / Referee, Watson Conference on Interaction between Architecture, Circuits, and Compilers. (2006).

Program Committee Member, IEEE International Symposium on Workload Characterization. (2005).

Program Committee Member, International Symposium on Code Generation and Optimization. (2005).

Reviewer / Referee, International Symposium on Code Generation and Optimization. (2005).

Reviewer / Referee, State Faculty Support Grant Program at California Polytechnic State University. (2005).

Session Chair, International Symposium on Code Generation and Optimization. (2005).

Reviewer / Referee, International Conference on Parallel Architectures and Compilation Techniques. (2001 - 2005).

Co-Founder and Organizer, Value-Prediction and Value-Based Optimization Workshop. (2003 - 2004).

Reviewer / Referee, National Science Foundation. (2003 - 2004).

Reviewer / Referee, Value-Prediction and Value-Based Optimization Workshop. (2003 - 2004).

Reviewer / Referee, IEEE Computer. (2003).
Additional Comments: 2004, 2006

Reviewer / Referee, Workshop on Novel Uses of System Area Networks. (2003).

Program Committee Member, Annual ACM International Conference on Supercomputing. (2002).

Reviewer / Referee, European Conference on Parallel Computing. (2001).

Reviewer / Referee, The Computer Journal. (2001).

Reviewer / Referee, Workshop on Caching, Coherence, and Consistency. (2001).

Reviewer / Referee, USENIX Annual Technical Conference. (1998).

C. Community:

Science Fair Judge, Canyon Ridge Middle School, Austin, TX. (January 2018).

Science Fair Judge, Canyon Ridge Middle School, Austin, TX. (January 2017).

Science Fair Judge, Canyon Ridge Middle School, Austin, TX. (January 2016).

Science Fair Judge, Canyon Ridge Middle School, Austin, TX. (January 2015).

Science Fair Judge, Canyon Ridge Middle School, Austin, TX. (January 2014).

D. Organization Memberships:

National Center for Women & Information Technology (NCWIT). (2015 - Present).

Association for Computing Machinery (ACM). (1998 - Present).

Institute of Electrical and Electronics Engineers (IEEE). (1997 - Present).

E. Service Honors and Awards:

Award / Honor Nominee: Recognition of Service Award, Association for Computing Machinery (ACM).
October 2004
June 2003