TEXAS STATE VITA

I. Academic/Professional Background

A. Name: Jeffrey Charles Stevens Title: Mr.

B. Educational Background

Degree	*Year*	*University*	*Major*
Master of Engineering	1985	Stevens Institute of Technology	Electrical Engineering

Thesis/Dissertation: n/a

Degree	*Year*	*University*	*Major*
Bachelor of Engineering	1982	Stevens Institute of Technology	Electrical Engineering

Thesis/Dissertation: n/a

C. University Experience

Position	*University*	*Dates*
Assistant Professor of Practice	Texas State University	August 2024 – present
Lecturer	Texas State University	Jan 2022 – August 2024

D. Relevant Professional Experience

Position	*Entity*	*Dates*
Manager/Director, Engineering	Hewlett-Packard	Mar 2002 – Mar 2020
Design Engineer/Manager	Compaq Computer Corp.	Jun 1988 – Feb 2002
Electrical Engineer	ITT Avionics	Jan 1982 – May 1988

E. Other Professional Credentials (licensure, certification, etc.)

Patent Awards:

Automated Verification of an Audio Sound Processing Solution	84618737 07 Apr 2017
Audio Privacy Mode	84618669 07 Apr 2017
Using an Address as a Snoop Invalidate Signal During Snoop Cycles	81497223 07 May 2002
Meeting time expiration indication on conference room solutions	84662986 02 Aug 2017
Dynamic Adjustment of MIC Tuning Parameters	84649770 13 Jul 2017
Adding a click sound to HP Skype collaborative buttons	84622827 20 Apr 2017
Dual Hard Drive Expansion Module	84279725 08 Jun 2015
DisplayMat	84224066 17 Apr 2015
Video Conference Flip Image	83928888 14 Apr 2014
Optimized Tower Configuration	82746408 16 Apr 2012

Dynamic power sense for PoE powered AiO Zero Client 82658087 02 Mar 2011
BIOS Setup Option to Allow User to Increase Minimum System Fan Speed 81516365 08 Jul 2004
Computer Fan Speed System to Reduce Audible Perceptibility of Fan Speed Changes 81498517 07 May 2002
Apparatus and Method for Dynamically Elevating a Lower-Level Bus Master to an Upper-Level Bus Master Within a Multi-Level Arbitration System 81498352 07 May 2002
Computer System with Bridge Logic that Includes an Internal Modular Expansion Bus and a Common Master Interface for Internal Master Devices 81498167 07 May 2002
Computer System with Bridge Logic that Includes an Internal Modular Expansion Bus and a Common Target Interface for Internal Target Devices 81498166 07 May 2002
Computer System with Adaptive Memory Arbitration Scheme 81498044 07 May 2002
Cache Memory Using Unique Burst Counter Circuitry and Asynchronous Interleaved RAM Banks for Zero Wait State Operation 81497461 07 May 2002
Method of Preventing Cache Corruption During Microprocessor Pipelined Burst Operations 81497396 07 May 2002
Interfacing Direct Memory Access Devices to a Non-ISA Bus 81497307 07 May 2002
Cache Memory System Which Snoops an Operation to a First Location in a Cache Line and Does Not Snoop Further Operations to Locations in the Same Line 81496914 07 May 2002
Multiprocessor Cache Snoop Access Protocol Wherein Snoop Means Performs Snooping Operations After Host Bus Cycle Completions & Delays Subsequent Host Bus Cycles Until… 81496616 07 May 2002
Dual-ported Cache Used With a 386-type Bus in a Multiprocessor Environment 81496614 07 May 2002
Method of Supporting Audio for KVM Extension in a Server Platform 81496477 07 May 2002
Solution for Integrating KVM Extension Transmitter with a Graphics Controller on a PCI Card 81496476 07 May 2002
Method of Connecting to a KVM Transmitter Using Internal Cables 81496465 07 May 2002

II. TEACHING

A. Teaching Honors and Awards: Part-Time Faculty Excellence in Teaching, 2024

B. Courses Taught:

Electrical Engineering Design I, EE 4390, Spring 2022 – Spring 2025
Electrical Engineering Design I, EE 4390, Fall 2022 – Spring 2025

C. Graduate Theses/Dissertations, Honors Theses, or Exit Committees (if supervisor, please indicate): none

D. Courses Prepared and Curriculum Development: none

E. Funded External Teaching Grants and Contracts: none

F. Submitted, but not Funded, External Teaching Grants and Contracts: none

G. Funded Internal Teaching Grants and Contracts: none

H. Submitted, but not Funded, Internal Teaching Grants and Contracts: none

I. Other:

III. SCHOLARLY/CREATIVE

A. Works in Print (including works accepted, forthcoming, in press)

1. Books (if not refereed, please indicate)

a. Scholarly Monographs: none

b. Textbooks: none

c. Edited Books: none

d. Chapters in Books: none

e. Creative Books: none

2. Articles

a. Refereed Journal Articles: none

b. Non-refereed Articles: none

3. Conference Proceedings

a. Refereed Conference Proceedings: none

b. Non-refereed: none

4. Abstracts: none

5. Reports: none

6. Book Reviews: none

7. Other Works in Print: none

B. Works not in Print

1. Papers Presented at Professional Meetings:
Co-author (1998). Device Bay: Device Bay Interface Specification, Revision 0.90, Compaq, Intel, Microsoft, November 6, 1998

2. Invited Talks, Lectures, and Presentations:

3. Consultancies: none

4. Workshops: none

5. Other Works not in Print:

a. Works “submitted” or “under review”: none

b. Works “ in progress”: none

c. Other works not in print: none

C. Grants and Contracts

1. Funded External Grants and Contracts: none

2. Submitted, but not Funded, External Grants and Contracts: none

3. Funded Internal Grants and Contracts: none

4. Submitted, but not Funded, Internal Grants and Contracts: none

D. Fellowships, Awards, Honors:

IV. SERVICE

A. Institutional

1. University:
Electrical Engineering Design I, EE 4390, Project Sponsor, Fall 2021, Spring 2022, Fall 2022

2. College: none

3. Department/School: none

B. Professional: none

C. Community: none

D. Service Honors and Awards: none

E. Service Grants and Contracts

1. Funded External Service Grants and Contracts: none

2. Submitted, but not Funded, External Service Grants and Contracts: none

3. Funded Internal Service Grants and Contracts: none

4. Submitted, but not Funded, Internal Service Grants and Contracts: none

Updated 6/2012